

CLAIMS

What is claimed is:

1. A half-rail differential driver circuit
5 comprising:
 a first supply voltage;
 a differential line pair, said differential line
pair comprising a first line terminal and a second line
terminal;
10 said first line terminal and said second line
terminal being shorted together during a pre-charge
phase of operation of said half-rail differential
driver circuit such that said first line terminal and
said second line terminal are charged to half said
15 first supply voltage.

2. A half-rail differential driver circuit
comprising:
20 a first supply voltage;
 at least one half-rail differential driver circuit
IN terminal and at least one half-rail differential
driver circuit INBAR terminal;
 at least one half-rail differential driver circuit
25 OUT terminal and at least one half-rail differential
driver circuit OUTBAR terminal; said at least one
half-rail differential driver circuit OUT terminal and
at least one half-rail differential driver circuit

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OUTBAR terminal forming a differential line pair,
wherein;

during a pre-charge phase of operation of said
half-rail differential driver circuit said at least one
5 half-rail differential driver circuit IN terminal and
said at least one half-rail differential driver circuit
INBAR terminal are shorted together such that said at
least one half-rail differential driver circuit IN
terminal and said at least one half-rail differential
10 driver circuit INBAR terminal are charged to half said
first supply voltage, further wherein;

during said pre-charge phase of operation of said
half-rail differential driver circuit said at least one
half-rail differential driver circuit OUT terminal and
15 said at least one half-rail differential driver circuit
OUTBAR terminal are shorted together such that said at
least one half-rail differential driver circuit OUT
terminal and said at least one half-rail differential
driver circuit OUTBAR terminal are charged to half said
20 first supply voltage.

3. A chain of half-rail differential driver
circuits comprising:

25 a first supply voltage;

a first half-rail differential driver circuit,
said first half-rail differential driver circuit
comprising:

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at least one first half-rail differential driver circuit IN terminal and at least one first half-rail differential driver circuit INBAR terminal;

5 at least one first half-rail differential driver circuit OUT terminal and at least one first half-rail differential driver circuit OUTBAR terminal; said at least one first half-rail differential driver circuit OUT terminal and at
10 least one first half-rail differential driver circuit OUTBAR terminal forming a differential line pair, wherein;

during a pre-charge phase of operation of said first half-rail differential driver circuit
15 said at least one first half-rail differential driver circuit IN terminal and said at least one first half-rail differential driver circuit INBAR terminal are shorted together such that said at least one first half-rail differential driver
20 circuit IN terminal and said at least one first half-rail differential driver circuit INBAR terminal are charged to half said first supply voltage, further wherein;

during said pre-charge phase of operation of
25 said first half-rail differential driver circuit said at least one first half-rail differential driver circuit OUT terminal and said at least one first half-rail differential driver circuit OUTBAR

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terminal are shorted together such that said at
least one first half-rail differential driver
circuit OUT terminal and said at least one first
half-rail differential driver circuit OUTBAR
terminal are charged to half said first supply
voltage; and
a second half-rail differential driver circuit

said second half-rail differential driver circuit
comprising:

at least one second half-rail differential
driver circuit IN terminal and at least one second
half-rail differential driver circuit INBAR
terminal, said at least one second half-rail
differential driver circuit IN terminal being
coupled to said first half-rail differential
driver circuit OUT terminal and said at least one
second half-rail differential driver circuit INBAR
terminal being coupled to said first half-rail
differential driver circuit OUTBAR terminal;

at least one second half-rail differential
driver circuit OUT terminal and at least one
second half-rail differential driver circuit
OUTBAR terminal; said at least one second half-
rail differential driver circuit OUT terminal and
at least one second half-rail differential driver
circuit OUTBAR terminal forming a differential
line pair, wherein;

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5 during a pre-charge phase of operation of
said second half-rail differential driver circuit
said at least one second half-rail differential
driver circuit IN terminal and said at least one
10 second half-rail differential driver circuit INBAR
terminal are shorted together such that said at
least one second half-rail differential driver
circuit IN terminal and said at least one second
half-rail differential driver circuit INBAR
15 terminal are charged to half said first supply
voltage, further wherein;

15 during said pre-charge phase of operation of
said second half-rail differential driver circuit
said at least one second half-rail differential
driver circuit OUT terminal and said at least one
20 second half-rail differential driver circuit
OUTBAR terminal are shorted together such that
said at least one second half-rail differential
driver circuit OUT terminal and said at least one
25 second half-rail differential driver circuit
OUTBAR terminal are charged to half said first
supply voltage.

25 4. A half-rail differential driver circuit
comprising:
a first supply voltage;
a second supply voltage;

a clock signal;
a half-rail differential driver circuit first IN
terminal;
a half-rail differential driver circuit second IN
5 terminal;
a half-rail differential driver circuit third IN
terminal;
a half-rail differential driver circuit fourth IN
terminal;
10 a half-rail differential driver circuit first
INBAR terminal;
a half-rail differential driver circuit second
INBAR terminal;
a half-rail differential driver circuit third
15 INBAR terminal;
a half-rail differential driver circuit fourth
INBAR terminal;
a half-rail differential driver circuit first
node;
20 a half-rail differential driver circuit second
node;
a half-rail differential driver circuit third
node;
a half-rail differential driver circuit fourth
25 node;
a first inverter, said first inverter having a
first inverter input terminal and a first inverter
output terminal, said first inverter input terminal

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being coupled to said half-rail differential driver circuit first node;

a second inverter, said second inverter having a second inverter input terminal and a second inverter output terminal, said second inverter input terminal being coupled to said half-rail differential driver circuit second node;

a third inverter, said third inverter having a third inverter input terminal and a third inverter output terminal, said third inverter input terminal being coupled to said half-rail differential driver circuit third node;

a fourth inverter, said fourth inverter having a fourth inverter input terminal and a fourth inverter output terminal, said fourth inverter input terminal being coupled to said half-rail differential driver circuit fourth node;

a half-rail differential driver circuit OUT terminal;

a half-rail differential driver circuit OUTBAR terminal;

a first transistor, said first transistor comprising a first transistor first flow electrode, a first transistor second flow electrode and a first transistor control electrode, said first transistor first flow electrode being coupled to said half-rail differential driver circuit first IN terminal, said first transistor second flow electrode being coupled to

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said half-rail differential driver circuit first node,
said first transistor control electrode being coupled
to said half-rail differential driver circuit first
INBAR terminal;
5 a second transistor, said second transistor
comprising a second transistor first flow electrode, a
second transistor second flow electrode, said second transistor
transistor control electrode being coupled to said first supply
10 first flow electrode being coupled to said half-rail differential driver
voltage, said second transistor second flow electrode
being coupled to said half-rail differential driver
circuit OUT terminal, said second transistor control
electrode being coupled to said first inverter output
terminal;
15 a third transistor, said third transistor
comprising a third transistor first flow electrode, a
third transistor second flow electrode and a third
transistor control electrode, said third transistor
20 first flow electrode being coupled to said second
supply voltage, said third transistor second flow
electrode being coupled to said half-rail differential
driver circuit first node, said third transistor
control electrode being coupled to said half-rail
25 differential driver circuit first INBAR terminal;
a fourth transistor, said fourth transistor
comprising a fourth transistor first flow electrode, a
fourth transistor second flow electrode and a fourth
transistor control electrode, said fourth transistor

first flow electrode being coupled to said first supply voltage, said fourth transistor second flow electrode being coupled to said half-rail differential driver circuit second node, said fourth transistor control electrode being coupled to said half-rail differential driver circuit second INBAR terminal;

a fifth transistor, said fifth transistor comprising a fifth transistor first flow electrode, a fifth transistor second flow electrode and a fifth transistor control electrode, said fifth transistor first flow electrode being coupled to said half-rail differential driver circuit second IN terminal, said fifth transistor second flow electrode being coupled to said half-rail differential driver circuit second node, said fifth transistor control electrode being coupled to said half-rail differential driver circuit second INBAR terminal;

a sixth transistor, said sixth transistor comprising a sixth transistor first flow electrode, a sixth transistor second flow electrode and a sixth transistor control electrode, said sixth transistor first flow electrode being coupled to said second supply voltage, said sixth transistor second flow electrode being coupled to said second transistor second flow electrode and said half-rail differential driver circuit OUT terminal, said sixth transistor control electrode being coupled to said second inverter out terminal;

a seventh transistor, said seventh transistor comprising a seventh transistor first flow electrode, a seventh transistor second flow electrode and a seventh transistor control electrode, said seventh transistor first flow electrode being coupled to said half-rail differential driver circuit OUT terminal, said seventh transistor second flow electrode being coupled to said half-rail differential driver circuit OUTBAR terminal, said seventh transistor control electrode being coupled to said clock signal;

an eighth transistor, said eighth transistor comprising a eighth transistor first flow electrode, a eighth transistor second flow electrode and a eighth transistor control electrode, said eighth transistor first flow electrode being coupled to said half-rail differential driver circuit third INBAR terminal, said eighth transistor second flow electrode being coupled to said half-rail differential driver circuit third node, said eighth transistor control electrode being coupled to said half-rail differential driver circuit third IN terminal;

a ninth transistor, said ninth transistor comprising a ninth transistor first flow electrode, a ninth transistor second flow electrode and a ninth transistor control electrode, said ninth transistor first flow electrode being coupled to said first supply voltage, said ninth transistor second flow electrode being coupled to said half-rail differential driver

circuit OUTBAR terminal, said ninth transistor control electrode being coupled to said third inverter output terminal;

a tenth transistor, said tenth transistor
5 comprising a tenth transistor first flow electrode, a tenth transistor second flow electrode and a tenth transistor control electrode, said tenth transistor first flow electrode being coupled to said second supply voltage, said tenth transistor second flow
10 electrode being coupled to said half-rail differential driver circuit third node, said tenth transistor control electrode being coupled to said half-rail differential driver circuit third IN terminal;

a eleventh transistor, said eleventh transistor
15 comprising a eleventh transistor first flow electrode, a eleventh transistor second flow electrode and a eleventh transistor control electrode, said eleventh transistor first flow electrode being coupled to said first supply voltage, said eleventh transistor second
20 flow electrode being coupled to said half-rail differential driver circuit fourth node, said eleventh transistor control electrode being coupled to said half-rail differential driver circuit fourth IN terminal;

25 a twelfth transistor, said twelfth transistor comprising a twelfth transistor first flow electrode, a twelfth transistor second flow electrode and a twelfth transistor control electrode, said twelfth transistor

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first flow electrode being coupled to said half-rail differential driver circuit fourth INBAR terminal, said twelfth transistor second flow electrode being coupled to said half-rail differential driver circuit fourth node, said twelfth transistor control electrode being coupled to said half-rail differential driver circuit fourth IN terminal;

a thirteenth transistor, said thirteenth transistor comprising a thirteenth transistor first flow electrode, a thirteenth transistor second flow electrode and a thirteenth transistor control electrode, said thirteenth transistor first flow electrode being coupled to said second supply voltage, said thirteenth transistor second flow electrode being coupled to said ninth transistor second flow electrode and said half-rail differential driver circuit OUTBAR terminal, said thirteenth transistor control electrode being coupled to said fourth inverter out terminal.

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5. The half-rail differential driver circuit of Claim 4, wherein;

said first supply voltage is VDD and said second supply voltage is ground.

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6. The half-rail differential driver circuit of Claim 5, wherein;

said first transistor, said second transistor,
said fourth transistor, said eighth transistor, said
ninth transistor and said eleventh transistor are
PFETs, further wherein;

5 said third transistor, said fifth transistor, said
sixth transistor, said seventh transistor, said tenth
transistor, said twelfth transistor and said thirteenth
transistor are NFETs.

10

7. A chain of half-rail differential driver
circuits comprising:

 a first supply voltage;
 a second supply voltage;
15 a clock signal;
 a first half-rail differential driver circuit,
said first half-rail differential driver circuit
comprising:
 a first half-rail differential driver circuit
20 first IN terminal;
 a first half-rail differential driver circuit
second IN terminal;
 a first half-rail differential driver circuit
third IN terminal;
25 a first half-rail differential driver
circuit fourth IN terminal;
 a first half-rail differential driver circuit
first INBAR terminal;

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a first half-rail differential driver circuit
second INBAR terminal;

a first half-rail differential driver circuit
third INBAR terminal;

5 a first half-rail differential driver circuit
fourth INBAR terminal;

a first half-rail differential driver circuit
first node;

10 a first half-rail differential driver circuit
second node;

a first half-rail differential driver circuit
third node;

a first half-rail differential driver circuit
fourth node;

15 a first inverter, said first inverter having
a first inverter input terminal and a first
inverter output terminal, said first inverter
input terminal being coupled to said first half-
rail differential driver circuit first node;

20 a second inverter, said second inverter
having a second inverter input terminal and a
second inverter output terminal, said second
inverter input terminal being coupled to said
first half-rail differential driver circuit second
25 node;

a third inverter, said third inverter having
a third inverter input terminal and a third
inverter output terminal, said third inverter

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input terminal being coupled to said first half-rail differential driver circuit third node;

a fourth inverter, said fourth inverter having a fourth inverter input terminal and a fourth inverter output terminal, said fourth inverter input terminal being coupled to said first half-rail differential driver circuit fourth node;

a first half-rail differential driver circuit OUT terminal;

a first half-rail differential driver circuit OUTBAR terminal;

a first transistor, said first transistor comprising a first transistor first flow electrode, a first transistor second flow electrode and a first transistor control electrode, said first transistor first flow electrode being coupled to said first half-rail differential driver circuit first IN terminal, said first transistor second flow electrode being coupled to said first half-rail differential driver circuit first node, said first transistor control electrode being coupled to said first half-rail differential driver circuit first INBAR terminal;

a second transistor, said second transistor comprising a second transistor first flow electrode, a second transistor second flow

electrode and a second transistor control
electrode, said second transistor first flow
electrode being coupled to said first supply
voltage, said second transistor second flow
5 electrode being coupled to said first half-rail
differential driver circuit OUT terminal, said
second transistor control electrode being coupled
to said first inverter output terminal;

a third transistor, said third transistor
10 comprising a third transistor first flow
electrode, a third transistor second flow
electrode and a third transistor control
electrode, said third transistor first flow
electrode being coupled to said second supply
15 voltage, said third transistor second flow
electrode being coupled to said first half-rail
differential driver circuit first node, said third
transistor control electrode being coupled to said
first half-rail differential driver circuit first
20 INBAR terminal;

a fourth transistor, said fourth transistor
comprising a fourth transistor first flow
electrode, a fourth transistor second flow
electrode and a fourth transistor control
25 electrode, said fourth transistor first flow
electrode being coupled to said first supply
voltage, said fourth transistor second flow
electrode being coupled to said first half-rail

differential driver circuit second node, said fourth transistor control electrode being coupled to said first half-rail differential driver circuit second INBAR terminal;

5 a fifth transistor, said fifth transistor comprising a fifth transistor first flow electrode, a fifth transistor second flow electrode and a fifth transistor control electrode, said fifth transistor first flow
10 electrode being coupled to said first half-rail differential driver circuit second IN terminal, said fifth transistor second flow electrode being coupled to said first half-rail differential driver circuit second node, said fifth transistor
15 control electrode being coupled to said first half-rail differential driver circuit second INBAR terminal;

 a sixth transistor, said sixth transistor comprising a sixth transistor first flow
20 electrode, a sixth transistor second flow electrode and a sixth transistor control electrode, said sixth transistor first flow electrode being coupled to said second supply voltage, said sixth transistor second flow
25 electrode being coupled to said second transistor second flow electrode and said first half-rail differential driver circuit OUT terminal, said

sixth transistor control electrode being coupled
to said second inverter out terminal;

5 a seventh transistor, said seventh transistor
comprising a seventh transistor first flow
electrode, a seventh transistor second flow
electrode and a seventh transistor control
electrode, said seventh transistor first flow
electrode being coupled to said first half-rail
differential driver circuit OUT terminal, said
10 seventh transistor second flow electrode being
coupled to said first half-rail differential
driver circuit OUTBAR terminal, said seventh
transistor control electrode being coupled to said
clock signal;

15 an eighth transistor, said eighth transistor
comprising a eighth transistor first flow
electrode, a eighth transistor second flow
electrode and a eighth transistor control
electrode, said eighth transistor first flow
20 electrode being coupled to said first half-rail
differential driver circuit third INBAR terminal,
said eighth transistor second flow electrode being
coupled to said first half-rail differential
driver circuit third node, said eighth transistor
25 control electrode being coupled to said first
half-rail differential driver circuit third IN
terminal;

a ninth transistor, said ninth transistor comprising a ninth transistor first flow electrode, a ninth transistor second flow electrode and a ninth transistor control electrode, said ninth transistor first flow electrode being coupled to said first supply voltage, said ninth transistor second flow electrode being coupled to said first half-rail differential driver circuit OUTBAR terminal, said ninth transistor control electrode being coupled to said third inverter output terminal;

a tenth transistor, said tenth transistor comprising a tenth transistor first flow electrode, a tenth transistor second flow electrode and a tenth transistor control electrode, said tenth transistor first flow electrode being coupled to said second supply voltage, said tenth transistor second flow electrode being coupled to said first half-rail differential driver circuit third node, said tenth transistor control electrode being coupled to said first half-rail differential driver circuit third IN terminal;

a eleventh transistor, said eleventh transistor comprising a eleventh transistor first flow electrode, a eleventh transistor second flow electrode and a eleventh transistor control electrode, said eleventh transistor first flow

electrode being coupled to said first supply
voltage, said eleventh transistor second flow
electrode being coupled to said first half-rail
differential driver circuit fourth node, said
5 eleventh transistor control electrode being
coupled to said first half-rail differential
driver circuit fourth IN terminal;

a twelfth transistor, said twelfth transistor
comprising a twelfth transistor first flow
10 electrode, a twelfth transistor second flow
electrode and a twelfth transistor control
electrode, said twelfth transistor first flow
electrode being coupled to said first half-rail
differential driver circuit fourth INBAR terminal,
15 said twelfth transistor second flow electrode
being coupled to said first half-rail differential
driver circuit fourth node, said twelfth
transistor control electrode being coupled to said
first half-rail differential driver circuit fourth
20 IN terminal;

a thirteenth transistor, said thirteenth
transistor comprising a thirteenth transistor
first flow electrode, a thirteenth transistor
second flow electrode and a thirteenth transistor
25 control electrode, said thirteenth transistor
first flow electrode being coupled to said second
supply voltage, said thirteenth transistor second
flow electrode being coupled to said ninth

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transistor second flow electrode and said first
half-rail differential driver circuit OUTBAR
terminal, said thirteenth transistor control
electrode being coupled to said fourth inverter
5 out terminal; and

a second half-rail differential driver circuit,
said second half-rail differential driver circuit
comprising:

a second half-rail differential driver
10 circuit first IN terminal coupled to said first
half-rail differential driver circuit OUT
terminal;

a second half-rail differential driver
circuit second IN terminal coupled to said first
15 half-rail differential driver circuit OUT
terminal;

a second half-rail differential driver
circuit third IN terminal coupled to said first
half-rail differential driver circuit OUT
20 terminal;

a second half-rail differential driver
circuit fourth IN terminal coupled to said first
half-rail differential driver circuit OUT
terminal;

a second half-rail differential driver
25 circuit first INBAR terminal coupled to said first
half-rail differential driver circuit OUTBAR
terminal;

a second half-rail differential driver
circuit second INBAR terminal coupled to said
first half-rail differential driver circuit OUTBAR
terminal;

5 a second half-rail differential driver
circuit third INBAR terminal coupled to said first
half-rail differential driver circuit OUTBAR
terminal;

10 a second half-rail differential driver
circuit fourth INBAR terminal coupled to said
first half-rail differential driver circuit OUTBAR
terminal;

a second half-rail differential driver
circuit first node;

15 a second half-rail differential driver
circuit second node;

a second half-rail differential driver
circuit third node;

20 a second half-rail differential driver
circuit fourth node;

a first inverter, said first inverter having
a first inverter input terminal and a first
inverter output terminal, said first inverter
input terminal being coupled to said second half-
25 rail differential driver circuit first node;

a second inverter, said second inverter
having a second inverter input terminal and a
second inverter output terminal, said second

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inverter input terminal being coupled to said
second half-rail differential driver circuit
second node;

5 a third inverter, said third inverter having
a third inverter input terminal and a third
inverter output terminal, said third inverter
input terminal being coupled to said second half-
rail differential driver circuit third node;

10 a fourth inverter, said fourth inverter
having a fourth inverter input terminal and a
fourth inverter output terminal, said fourth
inverter input terminal being coupled to said
second half-rail differential driver circuit
fourth node;

15 a second half-rail differential driver
circuit OUT terminal;

a second half-rail differential driver
circuit OUTBAR terminal;

20 a first transistor, said first transistor
comprising a first transistor first flow
electrode, a first transistor second flow
electrode and a first transistor control
electrode, said first transistor first flow
electrode being coupled to said second half-rail
25 differential driver circuit first IN terminal,
said first transistor second flow electrode being
coupled to said second half-rail differential
driver circuit first node, said first transistor

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control electrode being coupled to said second half-rail differential driver circuit first INBAR terminal;

5 a second transistor, said second transistor comprising a second transistor first flow electrode, a second transistor second flow electrode and a second transistor control electrode, said second transistor first flow electrode being coupled to said first supply
10 voltage, said second transistor second flow electrode being coupled to said second half-rail differential driver circuit OUT terminal, said second transistor control electrode being coupled to said first inverter output terminal;

15 a third transistor, said third transistor comprising a third transistor first flow electrode, a third transistor second flow electrode and a third transistor control electrode, said third transistor first flow electrode being coupled to said second supply
20 voltage, said third transistor second flow electrode being coupled to said second half-rail differential driver circuit first node, said third transistor control electrode being coupled to said
25 second half-rail differential driver circuit first INBAR terminal;

a fourth transistor, said fourth transistor comprising a fourth transistor first flow

electrode, a fourth transistor second flow
electrode and a fourth transistor control
electrode, said fourth transistor first flow
electrode being coupled to said first supply
5 voltage, said fourth transistor second flow
electrode being coupled to said second half-rail
differential driver circuit second node, said
fourth transistor control electrode being coupled
to said second half-rail differential driver
10 circuit second INBAR terminal;

a fifth transistor, said fifth transistor
comprising a fifth transistor first flow
electrode, a fifth transistor second flow
electrode and a fifth transistor control
15 electrode, said fifth transistor first flow
electrode being coupled to said second half-rail
differential driver circuit second IN terminal,
said fifth transistor second flow electrode being
coupled to said second half-rail differential
20 driver circuit second node, said fifth transistor
control electrode being coupled to said second
half-rail differential driver circuit second INBAR
terminal;

a sixth transistor, said sixth transistor
25 comprising a sixth transistor first flow
electrode, a sixth transistor second flow
electrode and a sixth transistor control
electrode, said sixth transistor first flow

electrode being coupled to said second supply
voltage, said sixth transistor second flow
electrode being coupled to said second transistor
second flow electrode and said second half-rail
5 differential driver circuit OUT terminal, said
sixth transistor control electrode being coupled
to said second inverter out terminal;

a seventh transistor, said seventh transistor
comprising a seventh transistor first flow
10 electrode, a seventh transistor second flow
electrode and a seventh transistor control
electrode, said seventh transistor first flow
electrode being coupled to said second half-rail
differential driver circuit OUT terminal, said
15 seventh transistor second flow electrode being
coupled to said second half-rail differential
driver circuit OUTBAR terminal, said seventh
transistor control electrode being coupled to said
clock signal;

20 an eighth transistor, said eighth transistor
comprising a eighth transistor first flow
electrode, a eighth transistor second flow
electrode and a eighth transistor control
electrode, said eighth transistor first flow
25 electrode being coupled to said second half-rail
differential driver circuit third INBAR terminal,
said eighth transistor second flow electrode being
coupled to said second half-rail differential

driver circuit third node, said eighth transistor control electrode being coupled to said second half-rail differential driver circuit third IN terminal;

5 a ninth transistor, said ninth transistor comprising a ninth transistor first flow electrode, a ninth transistor second flow electrode and a ninth transistor control electrode, said ninth transistor first flow
10 electrode being coupled to said first supply voltage, said ninth transistor second flow electrode being coupled to said second half-rail differential driver circuit OUTBAR terminal, said ninth transistor control electrode being coupled
15 to said third inverter output terminal;

 a tenth transistor, said tenth transistor comprising a tenth transistor first flow electrode, a tenth transistor second flow electrode and a tenth transistor control
20 electrode, said tenth transistor first flow electrode being coupled to said second supply voltage, said tenth transistor second flow electrode being coupled to said second half-rail differential driver circuit third node, said tenth
25 transistor control electrode being coupled to said second half-rail differential driver circuit third IN terminal;

a eleventh transistor, said eleventh transistor comprising a eleventh transistor first flow electrode, a eleventh transistor second flow electrode and a eleventh transistor control electrode, said eleventh transistor first flow electrode being coupled to said first supply voltage, said eleventh transistor second flow electrode being coupled to said second half-rail differential driver circuit fourth node, said eleventh transistor control electrode being coupled to said second half-rail differential driver circuit fourth IN terminal;

a twelfth transistor, said twelfth transistor comprising a twelfth transistor first flow electrode, a twelfth transistor second flow electrode and a twelfth transistor control electrode, said twelfth transistor first flow electrode being coupled to said second half-rail differential driver circuit fourth INBAR terminal, said twelfth transistor second flow electrode being coupled to said second half-rail differential driver circuit fourth node, said twelfth transistor control electrode being coupled to said second half-rail differential driver circuit fourth IN terminal;

a thirteenth transistor, said thirteenth transistor comprising a thirteenth transistor first flow electrode, a thirteenth transistor

second flow electrode and a thirteenth transistor control electrode, said thirteenth transistor first flow electrode being coupled to said second supply voltage, said thirteenth transistor second flow electrode being coupled to said ninth transistor second flow electrode and said second half-rail differential driver circuit OUTBAR terminal, said thirteenth transistor control electrode being coupled to said fourth inverter out terminal.

8. The chain of half-rail differential driver circuits of Claim 7, wherein;
said first supply voltage is VDD and said second supply voltage is ground.

9. The chain of half-rail differential driver circuits of Claim 8, wherein;
said first transistor, said second transistor, said fourth transistor, said eighth transistor, said ninth transistor and said eleventh transistor of said first half-rail differential driver circuit are PFETs, further wherein;

said first transistor, said second transistor, said fourth transistor, said eighth transistor, said ninth transistor and said eleventh transistor of said

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second half-rail differential driver circuit are PFETs,
further wherein;

said third transistor, said fifth transistor, said
sixth transistor, said seventh transistor, said tenth
5 transistor, said twelfth transistor and said thirteenth
transistor of said first half-rail differential driver
circuit are NFETs

said third transistor, said fifth transistor, said
sixth transistor, said seventh transistor, said tenth
10 transistor, said twelfth transistor and said thirteenth
transistor of said second half-rail differential driver
circuit are NFETs.

15 10. A method of half-rail differential driving
comprising:

providing a first supply voltage;

providing a differential line pair, said
differential line pair comprising a first line terminal
20 and a second line terminal, wherein;

said first line terminal and said second line
terminal are shorted together during a pre-charge phase
of operation of said half-rail differential driver
circuit such that said first line terminal and said
25 second line terminal are charged to half said first
supply voltage.

11. A method of half-rail differential driving
comprising:
providing a first supply voltage;
providing at least one half-rail differential
5 driver circuit IN terminal and at least one half-rail
differential driver circuit INBAR terminal;
providing at least one half-rail differential
driver circuit OUT terminal and at least one half-rail
differential driver circuit OUTBAR terminal, wherein;
10 said at least one half-rail differential driver
circuit OUT terminal and at least one half-rail
differential driver circuit OUTBAR terminal form a
differential line pair, further wherein;
during a pre-charge phase of operation, said at
15 least one half-rail differential driver circuit IN
terminal and said at least one half-rail differential
driver circuit INBAR terminal are shorted together such
that said at least one half-rail differential driver
circuit IN terminal and said at least one half-rail
20 differential driver circuit INBAR terminal are charged
to half said first supply voltage, further wherein;
during said pre-charge phase of operation, said at
least one half-rail differential driver circuit OUT
terminal and said at least one half-rail differential
25 driver circuit OUTBAR terminal are shorted together
such that said at least one half-rail differential
driver circuit OUT terminal and said at least one half-

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rail differential driver circuit OUTBAR terminal are charged to half said first supply voltage.

- 5 12. A method of providing a chain of half-rail differential driver circuits comprising:
- providing a first supply voltage;
- providing a first half-rail differential driver circuit, said first half-rail differential driver
- 10 circuit comprising:
- at least one first half-rail differential driver circuit IN terminal and at least one first half-rail differential driver circuit INBAR terminal;
- 15 at least one first half-rail differential driver circuit OUT terminal and at least one first half-rail differential driver circuit OUTBAR terminal; said at least one first half-rail differential driver circuit OUT terminal and at
- 20 least one first half-rail differential driver circuit OUTBAR terminal forming a differential line pair, wherein;
- during a pre-charge phase of operation of said first half-rail differential driver circuit
- 25 said at least one first half-rail differential driver circuit IN terminal and said at least one first half-rail differential driver circuit INBAR terminal are shorted together such that said at

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least one first half-rail differential driver
circuit IN terminal and said at least one first
half-rail differential driver circuit INBAR
terminal are charged to half said first supply
5 voltage, further wherein;

during said pre-charge phase of operation of
said first half-rail differential driver circuit
said at least one first half-rail differential
driver circuit OUT terminal and said at least one
10 first half-rail differential driver circuit OUTBAR
terminal are shorted together such that said at
least one first half-rail differential driver
circuit OUT terminal and said at least one first
half-rail differential driver circuit OUTBAR
15 terminal are charged to half said first supply
voltage; and

providing a second half-rail differential driver
circuit, said second half-rail differential driver
circuit comprising:

20 at least one second half-rail differential
driver circuit IN terminal and at least one second
half-rail differential driver circuit INBAR
terminal, said at least one second half-rail
differential driver circuit IN terminal being
25 coupled to said first half-rail differential
driver circuit OUT terminal and said at least one
second half-rail differential driver circuit INBAR

terminal being coupled to said first half-rail
differential driver circuit OUTBAR terminal;

at least one second half-rail differential
driver circuit OUT terminal and at least one
5 second half-rail differential driver circuit
OUTBAR terminal; said at least one second half-
rail differential driver circuit OUT terminal and
at least one second half-rail differential driver
circuit OUTBAR terminal forming a differential
10 line pair, wherein;

during a pre-charge phase of operation of
said second half-rail differential driver circuit
said at least one second half-rail differential
driver circuit IN terminal and said at least one
15 second half-rail differential driver circuit INBAR
terminal are shorted together such that said at
least one second half-rail differential driver
circuit IN terminal and said at least one second
half-rail differential driver circuit INBAR
20 terminal are charged to half said first supply
voltage, further wherein;

during said pre-charge phase of operation of
said second half-rail differential driver circuit
said at least one second half-rail differential
25 driver circuit OUT terminal and said at least one
second half-rail differential driver circuit
OUTBAR terminal are shorted together such that
said at least one second half-rail differential

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driver circuit OUT terminal and said at least one
second half-rail differential driver circuit
OUTBAR terminal are charged to half said first
supply voltage.

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